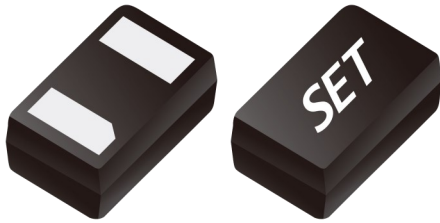


ESD Protection Diodes

Low Capacitance ESD and Transient Voltage Protection

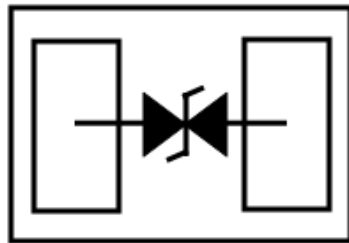
SD1205F10L DFN1006



Description

SD1205F10L is a low-capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for data, control or power lines. With maximum capacitance of 15 pF only, SD1205F10L is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4 (± 15 kV air, ± 8 kV contact discharge), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

Pinout and Functional Block Diagram



SD1205F10L uses ultra-small DFN1006 package. Each SD1205F10L device can protect one data line. It offers system designers flexibility to protect single data line where space is a premium concern.

Applications

- Serial and Parallel Ports
- Notebooks, Desktops, Servers
- Projection TV
- Cellular handsets and accessories
- Portable instrumentation
- Peripherals

Features

- IEC61000-4-2 (ESD) ± 15 kV (Air), ± 8 kV (Contact)
- IEC61000-4-4 (EFT) 40 A (5 / 50 ns)
- IEC61000-4-5 (Lighting) 5 A (8 / 20 μ s)
- 150 Watts Peak Pulse Power Per (tp=8 / 20 μ s)
- Low Capacitance: 15 pF (Maximum)
- Low Leakage Current
- Low Clamping Voltage
- Halogen Free and RoHS Compliant
- Flammability Rating: UL 94 V-0

Order Information

Type	Package	Marking	Size (mm)	Delivery Form	Delivery Quantity
SD1205F10L	DFN 1006	MOC	1.00 x 0.60 x 0.50	7" T&R	10000 PCS

Limiting Values

(T_A = 25 °C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{ESD}	Electrostatic Discharge Voltage	IEC 61000-4-2; Contact Discharge	-	20	kV
		IEC 61000-4-2; Air Discharge	-	25	kV
P _{PP}	Peak Pulse Power (8 / 20 μ s)	I _{PP} =5.0 A, t _p =8 / 20 μ s	-	150	W
T _A	Operating Temperature Range	-	-55	150	°C
T _{stg}	Storage Temperature Range	-	-55	150	°C

ESD Protection Diodes

Low Capacitance ESD and Transient Voltage Protection

SD1205F10L

DFN1006

Electrical Characteristics

($T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{RWM}	Reverse Working Voltage	$T_A = 25\text{ }^\circ\text{C}$	-	-	12	V
V_{BR}	Breakdown Voltage	$I_R = 1\text{ mA}$; $T_A = 25\text{ }^\circ\text{C}$	13.3	-	32	V
I_R	Reverse Leakage Current	$V_{RWM} = 12\text{ V}$; $T_A = 25\text{ }^\circ\text{C}$	-	-	0.2	μA
V_C	Clamping Voltage	$I_{PP} = 1\text{ A}$, $T_p = 8 / 20\text{ }\mu\text{s}$	-	-	19	V
		$I_{PP} = 5.0\text{ A}$, $T_p = 8 / 20\text{ }\mu\text{s}$	-	-	26	V
C_J	Junction Capacitance	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$	-	13	15	pF

Performance Curve for Reference

($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

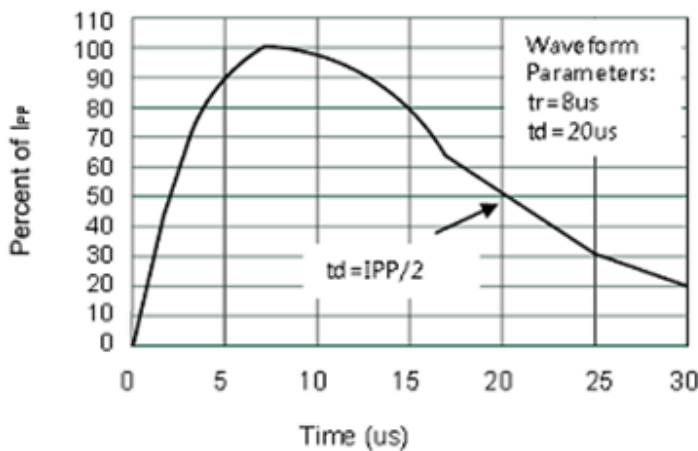


FIGURE 1
Pulse Waveform

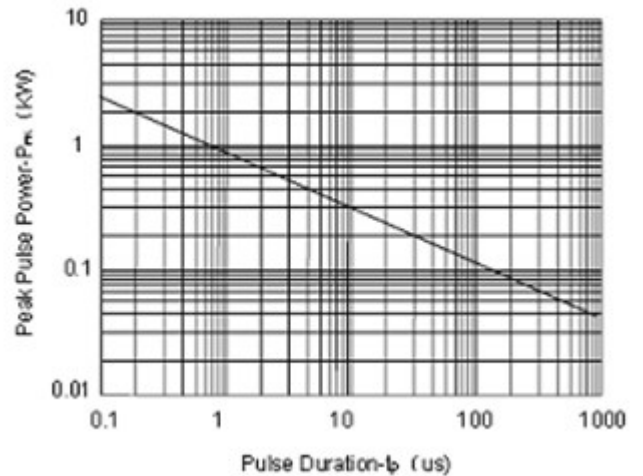


FIGURE 2
Non-Repetitive Peak Pulse Power VS. Pulse Time

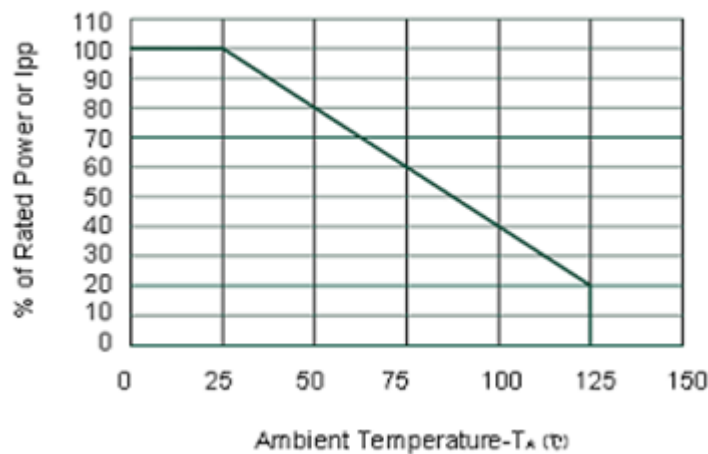


FIGURE 3
Power Derating Curve

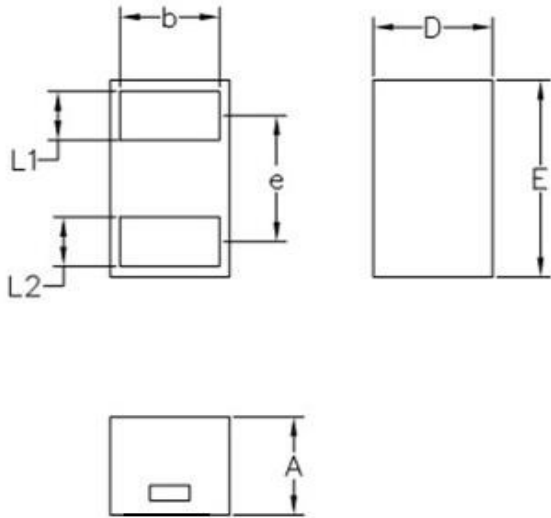
ESD Protection Diodes

Low Capacitance ESD and Transient Voltage Protection

SD1205F10L

DFN1006

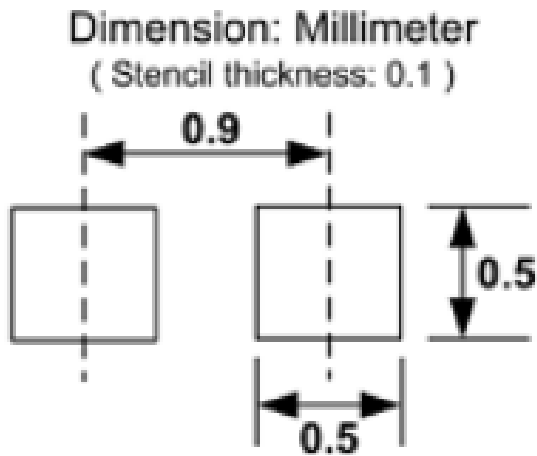
Package Dimensions - DFN1006



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
D	0.55	0.65	0.022	0.026
E	0.95	1.05	0.037	0.041
L1	0.20	0.30	0.008	0.012
L2	0.20	0.30	0.008	0.012
A	0.45	0.55	0.018	0.022
b	0.45	0.55	0.018	0.022
e	0.64 BSC		0.025 BSC	

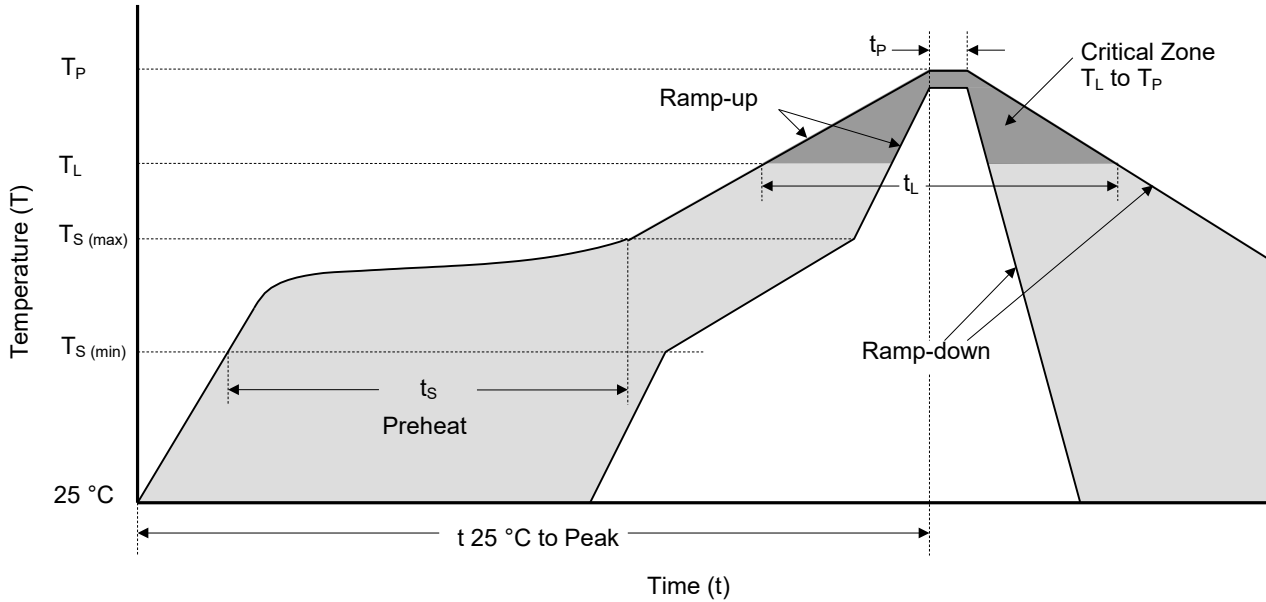
Recommended Solder Pad Footprint

(Ratings at 25 °C ambient temperature unless otherwise specified.)



Soldering Footprint

Soldering Parameters



Reflowing Condition

Reflow Soldering Parameters		Lead-Free Assembly
Pre-heat	Temperature Min ($T_{S (min)}$)	150 °C
	Temperature Max ($T_{S (max)}$)	200 °C
	Time (min to max) (t_s)	60 ~ 120 seconds
Average Ramp Up Rate (Liquidus Temp (T_L) to Peak)		3 °C / second max.
$T_S (max)$ to T_L Ramp-up Rate		3 °C / second max.
Reflow	Temperature (T_L) (Liquidus)	217 °C
	Time (min to max) (t_L)	60 ~ 150 seconds
Peak Temperature (T_P)		260 ^{+0/-5} °C
Time of within 5 °C of Actual Peak Temperature (t_P)		20 ~ 40 seconds
Ramp-down Rate		6 °C / second max.
Time from 25 °C to Peak Temperature		8 Minutes max.
Do Not Exceed		260 °C



ATTENTION

Usage

1. TVS must be operated in the specified ambient temp.
2. Do not clean the TVS with strong polar solvent such as ketone, esters, benzene and halogenated hydrocarbon, to avoid damaging the encapsulating layer.
3. Please do not apply severe vibration, shock or pressure to TVS, to avoid element cracking.

Replacement

1. If TVS is visually damaged, please replace it.
2. TVS is a non-repairable product. For safety sake, please use equivalent TVS for replacement.

Storage

1. Storage Temp. Range: (-55 to 150) °C.
2. Do not store the TVS at the high temp., high humidity or corrosive gas environment, to avoid influencing the solder- ability of the lead wires. The product shall be used up within 1 year after receiving the goods.

Environmental Conditions













































1. TVS should not be exposed to the open air, nor direct sunshine.
2. TVS should avoid rain, water vapor or other condition of high temp. and high humidity.
3. TVS should avoid sand dust, salt mist, or other harmful gases.

Max. Typical Capacitance of TVS

The typical capacitance of TVS is listed in the specifications. Designers may refer to it when designing TVS in High frequency circuit.

Installation Mechanical Stress

1. Do not knock TVS when installing, to avoid mechanical damage.
2. Please do not apply severe vibration, shock or pressure to TVS, to avoid surface resin or element cracking.

Package Outline					Circuit Diagram					
										
DFN0603	DFN1006	DFN1006-3L	DFN1610	DFN2020-3L	1CH/UNI	1CH/BI	2CH/UNI	2CH/BI	1CH/BI	1CH/UNI
										
DFN1610-6L	DFN2010-8L	DFN2510	DFN2626-10L	DFN3810-9L	1CH/UNI	1CH/BI	1CH/UNI	1CH/BI	2CH/UNI	2CH/BI
										
SOD-923	SOD-523	SOD-323	SOD-123	SOT-143	1CH/UNI	2CH/UNI	2CH/UNI	4CH/UNI	5CH/UNI	4CH/UNI
										
SOT-523	SOT-323	SOT-23	SOT-363	SOT-23-6L	2CH/BI	4CH/UNI	4CH/UNI	8CH/UNI	8CH/UNI	8CH/UNI